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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/921,423	08/02/2001	Randhir P.S. Thakur	3978.1US (95-0064.1)	8029
24247	7590	05/10/2004	EXAMINER	
TRASK BRITT P.O. BOX 2550 SALT LAKE CITY, UT 84110			MONDT, JOHANNES P	
			ART UNIT	PAPER NUMBER
			2826	

DATE MAILED: 05/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/921,423

Applicant(s)

THAKUR ET AL.A

Examiner

Johannes P Mondt

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 24 February 2004.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-9,11 and 12 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-9,11 and 12 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>12/29/03</u> . | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Information Disclosure Statement***

The examiner has considered the items listed on the Information Disclosure Statement filed 12/29/2003 and a signed copy of Form PTO-1449 is herewith enclosed.

### ***Response to Arguments***

Applicant's arguments in Applicant's Response filed 2/24/2004 have been fully considered but they are not persuasive. In particular, Applicant's allegation that "there is no motivation or suggestion in the Hsia reference or the other cited references to modulate the composition as in the present invention of claims 1 through 9 and 11 through 12" is left unsubstantiated while the previous Office Action mailed 11/19/2003 explained that the *only issue at hand* is the lack of teaching of the specification of the *particular kinds* of first and second oxides of different etch rates in Hsia et al (see page 4 of said Office Action), and that in this regard it was noted in said Office Action that it had long been known in the semiconductor device art of Applicant's invention (semiconductor device capacitors) (a) that BPSG is a standard material selection for capacitor sidewalls with reference to Ando column 2, lines 1-14 in which he teaches the use of BPSG as a capacitor sidewall insulator in a method including the etching thereof for self-alignment, and (b) that it has been known through Haller et al in the same art for years that the etch rate of BPSG can be markedly varied by doping BPSG with germanium, with specific reference to the abstract and column 2, lines 65-67 (inter alia the statements that "germanium concentration of 5% to 25% provides the preferred increased selectivity of the etch"), column 3, lines 17-24, that in particular refers to

Figure 2 showing the functional dependence in the etch rate of BPSG as a function of Ge-doping percentage. It follows from (a) and (b) that a standard selection of doped Ge BPSG layers for the first oxide and second oxide would have been obvious to one of ordinary skills in the art. Applicant is reminded in this regard that it has been held that mere selection of known materials generally understood to be suitable to make a device, the selection of the particular material being on the basis of suitability for the intended use, would be entirely obvious. In re Leshin 125 USPQ 416.

Furthermore, Applicant's allegation that modifying "the Hsia reference to modulate the composition in each layer, would alter the fundamental process that the corrugated structure is formed (sic)." No explanation is given by Applicant to support said allegation. While it is not entirely clear from the structure of this sentence what Applicant means, said sentence is interpreted to mean "modifying the Hsia reference to modulate the composition in each layer, would alter the fundamental process *in which* the corrugated structure is formed". But the modification is only a matter of material selection, while the process is entirely feasible through alternating graded doping, whereas only the device and not the process of making the device is applied for through the claims.

Next, Applicant alleges that Hsia et al teach away by maintaining the composition of each layer to be the same. However, in response to this allegation examiner points out herewith that layers 62 and 64 are formed of silicate glass (Hsia et al, column 4, lines 49-57), which, parenthetically is a broader term of BPSG, said layers 62 and 64 distinguished from each other by having different etch rates, and therefore the

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statement that layers 62 and 64 inherently must have different compositions follows from a proof *ad absurdum*: identical compositions necessarily result in identical sets of physical and chemical properties. The different compositions in Hsia et al result from different methods of making, i.e., plasma CVD and thermal CVD. However, this is irrelevant to the conclusion of different compositions.

In view the conclusion by Applicant of "impermissible hindsight based solely upon the Applicants' disclosure", based as it is on the above allegations, is not persuasive.

The final argument by Applicant that "if the Ando reference is assumed to teach side-wall capacitor structures formed from BPSG, any combination of the cited references might and would result in replacing the layers of silicon dioxide in the Hsia et al reference with layers of BPSG having a modulated density while the composition of each layer remains constant" is defective in several respects: (1) no assumption concerning the teaching of BPSG sidewall capacitor structures by Ando needs to be made, because Ando teaches exactly this (Ando, loc. cit.); (2) replacement of the oxide layers in Hsia et al following Ando and Haller does not necessarily amount in replacement of silicon oxide, - although there would be nothing incorrect about that, as a material embodiment teaches silicate glass for said oxide layers (column 4, line 54), while (3) the compositions of the two alternating layers following Ando and Haller necessarily are different because of the argument given in the paragraph just above.

All other arguments in traverse made by Applicant depend exclusively on the arguments of traverse discussed above.

In view of this, the examiner has no choice but to let the rejections made in the previous Office Action stand.

***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. ***Claim 1 is rejected*** under 35 U.S.C. 103(a) as being unpatentable over Hsia et al (5,827,783) in view of Ando (6,097,053) and Haller et al (5,804,506). With reference to Figs. 6-8: Hsia et al teach a semiconductor memory device (cf. column 1, line 6 and column 4, lines 12-13) having at least one memory cell having a capacitor cell (cf. column 2, line 60-62) formed of multiple layers of glass, said capacitor cell having a sidewall surface (cf. Figure 5-8), comprising:

at least one layer of a nonconductive oxide with a first etch rate 62 (cf. column 5, lines 33-35);

at least one layer of a nonconductive oxide with a second etch rate 64 (cf. column 4, line 66 – column 5, line 1);

said nonconductive oxide layer with second etching rate having a portion contacting at least a portion of said at least one layer of nonconductive oxide with first etching rate (see abutting layers 62 and 64 in Figure 7 in Hsia);

at least one layer 26 (cf. Figure 5 and col. 2, l. 2) of dielectric material (polysilicon is a dielectric material) covering at least the sidewall surface of the said capacitor cell; and

at least one electrode layer 28 (cf. col. 2, l. 1-11) deposited over at least a portion of the at least one layer of dielectric material.

*Hsia et al do not necessarily teach* the nonconductive oxide with first etch rate to be boro-phospho silicate glass and the nonconductive oxide with second etch rate to be germanium boro-phospho silicate glass. However, the use of boro-phospho silicate glass (BPSG) is a standard choice for the side wall in capacitors in the semiconductor device art as evidenced by the description of the prior art by Ando (cf. col. 2, l. 1-14 and Figure 4; in particular BPSG side wall 24, cf. col. 2, l. 4), while it has been known for years that germanium doping of boro-phospho silicate glass markedly increases the etch rate (both wet and dry) of boro-phospho silicate glass, as witnessed by Haller (Abstract, fifth and sixth sentence; column 2, lines 65-67, and column 3, lines 17-24; cf. also Figs. 2 and 3).

*Therefore, it would have been obvious* to one of ordinary skills in the art to modify the invention by Hsia et al at the time it was made so as to select boro-phospho silicate glass ( $B_2O_3 - P_2O_5 - SiO_2$ , hence a nonconductive oxide) for the aforementioned at least one layer 62, and to select germanium boro-phospho silicate glass (also a nonconductive oxide) for the aforementioned at least one layer 64.

Applicant is reminded in this regard that it has been held that mere selection of known materials generally understood to be suitable to make a device, the selection of

the particular material being on the basis of suitability for the intended use, would be entirely obvious. In re Leshin 125 USPQ 416.

3. ***Claim 2 is rejected*** under 35 U.S.C. 103(a) as being unpatentable over Hsia et al (5,827,783) in view of Ando (6,097,053) and Haller et al (5,804,506). With reference to Figs. 6-8: Hsia et al teach a semiconductor memory device (cf. column 1, line 6 and column 4, lines 12-13) having at least one memory cell having a capacitor cell (cf. column 2, line 60-62) formed of multiple layers of glass, said capacitor cell having a sidewall surface (cf. Figure 5-8), comprising:

- a plurality of layers of a nonconductive oxide with a first etch rate 62 (cf. column 5, lines 33-35);

- a plurality of layers of a nonconductive oxide with a second etch rate 64 (cf. column 4, line 66 – column 5, line 1);

- at least a portion of at least one layer of said plurality of nonconductive oxide layers with second etching rate contacting at least a portion of at least one layer of said plurality of nonconductive oxide with first etching rate (cf. Figs. 6-8);

- at least one layer 26 (cf. Figure 5 and col. 2, l. 2) of dielectric material (polysilicon is a dielectric material) covering at least the sidewall surface of the said capacitor cell; and

- at least one electrode layer 28 (cf. col. 2, l. 1-11) deposited over at least a portion of the at least one layer of dielectric material.



Hsia et al do not necessarily teach the nonconductive oxide with first etch rate to be boro-phospho silicate glass and the nonconductive oxide with second etch rate to be germanium boro-phospho silicate glass. However, the use of boro-phospho silicate glass (BPSG) is a standard choice for the side wall in capacitors in the semiconductor device art as evidenced by Ando, while BPSG is known for ease of deposition at relatively low temperature, reduced stress, and relatively low glass flow temperatures, while it has been known for years that germanium doping of boro-phospho silicate glass markedly increases the etch rate (both wet and dry) of boro-phospho silicate glass, as witnessed by Haller (Abstract, fifth and sixth sentence; column 2, lines 65-67, and column 3, lines 17-24; cf. also Figs. 2 and 3).

*Therefore, it would have been obvious* to one of ordinary skills in the art to modify the invention by Hsia et al at the time it was made so as to select boro-phospho silicate glass ( $B_2O_3 - P_2O_5 - SiO_2$ , hence a nonconductive oxide) for the aforementioned at nonconductive oxide 62, and to select germanium boro-phospho silicate glass (also a nonconductive oxide) for the aforementioned nonconductive 64.

Applicant is reminded in this regard that it has been held that mere selection of known materials generally understood to be suitable to make a device, the selection of the particular material being on the basis of suitability for the intended use, would be entirely obvious. In re Leshin 125 USPQ 416.

4. **Claim 3 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Hsia et al (5,827,783) in view of Ando (6,097,053) and Haller et al (5,804,506). With reference to

Figs. 6-8: Hsia et al teach a semiconductor memory device (cf. column 1, line 6 and column 4, lines 12-13) having at least one memory cell having a capacitor cell (cf. column 2, line 60-62) formed of multiple layers of glass, said capacitor cell having a sidewall surface (cf. Figure 5-8), comprising:

- a plurality of layers of a nonconductive oxide (with a first etch rate) 62 (cf. column 5, lines 33-35);

- a plurality of layers of a nonconductive oxide (with a second etch rate) 64 (cf. column 4, line 66 – column 5, line 1);

- each layer of said plurality of layers 64 having at least a portion thereof contacting at least a portion of at least one layer of said plurality of layers 62 (cf. Figs. 6-8).

Hsia et al do not necessarily teach the nonconductive oxide layers 62 to be boro-phospho silicate glass and the nonconductive oxide layers 64 to be germanium boro-phospho silicate glass. However, the use of boro-phospho silicate glass (BPSG) is a standard choice for capacitor side walls in the semiconductor device art as evidenced by the description of the prior art by Ando (cf. Fig. 4, col. 2, l. 1-14) while PBSG is well known for its ease of deposition at relatively low temperature, reduced stress, and relatively low glass flow temperatures, while it has been known for years that germanium doping of boro-phospho silicate glass markedly increases the etch rate (both wet and dry) of boro-phospho silicate glass, as witnessed by Haller (Abstract, fifth and sixth sentence; column 2, lines 65-67, and column 3, lines 17-24; cf. also Figs. 2 and 3).

*Therefore, it would have been obvious* to one of ordinary skills in the art to modify the invention by Hsia et al at the time it was made so as to select boro-phospho silicate glass ( $B_2O_3 - P_2O_5 - SiO_2$ , hence a nonconductive oxide) for the aforementioned at nonconductive oxide layers 62, and to select germanium boro-phospho silicate glass (also a nonconductive oxide) for the aforementioned nonconductive layers 64.

Applicant is reminded in this regard that it has been held that mere selection of known materials generally understood to be suitable to make a device, the selection of the particular material being on the basis of suitability for the intended use, would be entirely obvious. In re Leshin 125 USPQ 416.

5. **Claim 4** is rejected under 35 U.S.C. 103(a) as being unpatentable over Hsia et al (5,827,783) in view of Ando (6,097,053) and Haller et al (5,804,506). With reference to Figs. 6-8: Hsia et al teach a semiconductor memory device (cf. column 1, line 6 and column 4, lines 12-13) having at least one memory cell having a capacitor cell (cf. column 2, line 60-62) formed of multiple layers of glass, said capacitor cell having a sidewall surface (cf. Figure 5-8), comprising:

at least one layer of a nonconductive oxide (with a first etch rate) 62 (cf. column 5, lines 33-35);

at least one layer of a nonconductive oxide (with a second etch rate) 64 (cf. column 4, line 66 – column 5, line 1) having at least a portion thereof contacting at least a portion of said at least one layer 62 (cf. Figs. 6-8).

*Hsia et al do not necessarily teach* the nonconductive oxide layers 62 to be boro-phospho silicate glass and the nonconductive oxide layers 64 to be germanium boro-phospho silicate glass. However, the use of boro-phospho silicate glass (BPSG) is a standard choice for the side wall material in capacitors in the semiconductor device art as evidenced by Ando, while being known for its ease of deposition at relatively low temperature, reduced stress, and relatively low glass flow temperatures, and, furthermore, it has been known for years that germanium doping of boro-phospho silicate glass markedly increases the etch rate (both wet and dry) of boro-phospho silicate glass, as witnessed by Haller (Abstract, fifth and sixth sentence; column 2, lines 65-67, and column 3, lines 17-24; cf. also Figs. 2 and 3).

*Therefore, it would have been obvious* to one of ordinary skills in the art to modify the invention by Hsia et al at the time it was made so as to select boro-phospho silicate glass ( $B_2O_3 - P_2O_5 - SiO_2$ , hence a nonconductive oxide) for the aforementioned at nonconductive oxide layers 62, and to select germanium boro-phospho silicate glass (also a nonconductive oxide) for the aforementioned nonconductive layers 64.

Applicant is reminded in this regard that it has been held that mere selection of known materials generally understood to be suitable to make a device, the selection of the particular material being on the basis of suitability for the intended use, would be entirely obvious. In re Leshin 125 USPQ 416.

6. **Claim 5 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Hsia et al (5,827,783) in view of Ando (6,097,053) and Haller et al (5,804,506). With reference to

Figs. 6-8: Hsia et al teach a semiconductor memory device (cf. column 1, line 6 and column 4, lines 12-13) having at least one memory cell having a capacitor cell (cf. column 2, line 60-62) formed of multiple layers of glass, said capacitor cell having a sidewall surface (cf. Figure 5-8), comprising:

a plurality of layers of a nonconductive oxide (with a first etch rate) 62 (cf. column 5, lines 33-35);

a plurality of layers of a nonconductive oxide (with a second etch rate) 64 (cf. column 4, line 66 – column 5, line 1) at least a portion of at least one layer of said plurality of layers 64 contacting at least a portion of at least one layer of said plurality of layers 62 (cf. Figs. 6-8);

at least one layer 26 (cf. Figure 5 and col. 2, l. 2) of dielectric material (polysilicon is a dielectric material) covering at least the sidewall surface of the said capacitor cell; and

at least one electrode layer 28 (cf. col. 2, l. 1-11) deposited over at least a portion of the at least one layer of dielectric material.

*Hsia et al do not necessarily teach* the nonconductive oxide layers 62 to be boro-phospho silicate glass and the nonconductive oxide layers 64 to be germanium boro-phospho silicate glass. However, the use of boro-phospho silicate glass (BPSG) as the material for capacitor side walls in the semiconductor device art is well known as evident from the description of the prior art in Ando (cf. Fig. 4, col. 2, l. 1-14), while BPSG is widely known for its ease of deposition at relatively low temperature, reduced stress, and relatively low glass flow temperatures. Furthermore, it has been known for

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years that germanium doping of boro-phospho silicate glass markedly increases the etch rate (both wet and dry) of boro-phospho silicate glass, as witnessed by Haller (Abstract, fifth and sixth sentence; column 2, lines 65-67, and column 3, lines 17-24; cf. also Figs. 2 and 3).

*Therefore, it would have been obvious* to one of ordinary skills in the art to modify the invention by Hsia et al at the time it was made so as to select boro-phospho silicate glass ( $B_2O_3 - P_2O_5 - SiO_2$ , hence a nonconductive oxide) for the aforementioned at nonconductive oxide layers 62, and to select germanium boro-phospho silicate glass (also a nonconductive oxide) for the aforementioned nonconductive layers 64.

Applicant is reminded in this regard that it has been held that mere selection of known materials generally understood to be suitable to make a device, the selection of the particular material being on the basis of suitability for the intended use, would be entirely obvious. In re Leshin 125 USPQ 416.

7. **Claim 6** is rejected under 35 U.S.C. 103(a) as being unpatentable over Hsia et al (5,827,783) in view of Ando (6,097,053) and Haller et al (5,804,506). With reference to Figs. 6-8: Hsia et al teach a semiconductor memory device (cf. column 1, line 6 and column 4, lines 12-13) having at least one memory cell having a capacitor cell (cf. column 2, line 60-62) formed of multiple layers of glass, said capacitor cell having a sidewall surface (cf. Figure 5-8), comprising:

a plurality of layers of a nonconductive oxide (with a first etch rate) 62 (cf. column 5, lines 33-35);

a plurality of layers of a nonconductive oxide (with a second etch rate) 64 (cf. column 4, line 66 – column 5, line 1), each layer of said plurality of layers 64 having at least a portion thereof contacting at least a portion of at least one layer of said plurality of layers 62 (cf. Figs. 6-8);

at least one layer 26 (cf. Figure 5 and col. 2, l. 2) of dielectric material (polysilicon is a dielectric material) covering at least the sidewall surface of the said capacitor cell; and

at least one electrode layer 28 (cf. col. 2, l. 1-11) deposited over at least a portion of the at least one layer of dielectric material.

*Hsia et al do not necessarily teach* the nonconductive oxide layers 62 to be borophospho silicate glass and the nonconductive oxide layers 64 to be germanium borophospho silicate glass. However, the use of borophospho silicate glass (BPSG) as capacitor side wall material is standard in the semiconductor device art as evidenced by the description of the prior art in Ando, while PSGB is widely known for its ease of deposition at relatively low temperature, reduced stress, and relatively low glass flow temperatures. Furthermore, it has been known for years that germanium doping of borophospho silicate glass markedly increases the etch rate (both wet and dry) of borophospho silicate glass, as witnessed by Haller (Abstract, fifth and sixth sentence; column 2, lines 65-67, and column 3, lines 17-24; cf. also Figs. 2 and 3).

*Therefore, it would have been obvious* to one of ordinary skills in the art to modify the invention by Hsia et al at the time it was made so as to select borophospho silicate glass ( $B_2O_3 - P_2O_5 - SiO_2$ , hence a nonconductive oxide) for the aforementioned at

nonconductive oxide layers 62, and to select germanium boro-phospho silicate glass (also a nonconductive oxide) for the aforementioned nonconductive layers 64.

Applicant is reminded in this regard that it has been held that mere selection of known materials generally understood to be suitable to make a device, the selection of the particular material being on the basis of suitability for the intended use, would be entirely obvious. In re Leshin 125 USPQ 416.

8. ***Claim 7*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Hsia et al (5,827,783) in view of Ando (6,097,053) and Haller et al (5,804,506). With reference to Figs. 7 and 8: Hsia et al teach a semiconductor memory device (cf. column 1, line 6 and column 4, lines 12-13) having at least one memory cell having a capacitor cell (cf. column 2, line 60-62) formed of multiple layers of glass, said capacitor cell having a sidewall surface (cf. Figure 5-8), comprising:

at least one capacitor cell 78 (cf. column 6, line 47) having a portion thereof formed by at least one layer of nonconductive oxide 62 (cf. column 5, lines 33-35) and at least one layer of non-conductive oxide 64 (cf. column 4, line 66 – column 5, line 1) having at least a portion thereof contacting at least a portion of said at least one layer of nonconductive oxide 62;

at least one layer 26 (cf. Figure 5 and col. 2, l. 2) of dielectric material (polysilicon is a dielectric material) covering at least the sidewall surface of the said capacitor cell; and



at least one electrode layer 28 (cf. col. 2, l. 1-11) deposited over at least a portion of the at least one layer of dielectric material.

*Hsia et al do not necessarily teach* the nonconductive oxide layers 62 to be borophospho silicate glass and the nonconductive oxide layers 64 to be germanium borophospho silicate glass. However, the use of borophospho silicate glass (BPSG) is a standard choice for the side wall material in capacitors in the semiconductor device art as evidenced by the description of the prior art by Ando (cf. Fig. 4, col. 2, l. 1-14) while BPSG is widely known for its ease of deposition at relatively low temperature, reduced stress, and relatively low glass flow temperatures. Furthermore, it has been known for years that germanium doping of borophospho silicate glass markedly increases the etch rate (both wet and dry) of borophospho silicate glass, as witnessed by Haller (Abstract, fifth and sixth sentence; column 2, lines 65-67, and column 3, lines 17-24; cf. also Figs. 2 and 3).

*Therefore, it would have been obvious* to one of ordinary skills in the art to modify the invention by Hsia et al at the time it was made so as to select borophospho silicate glass ( $B_2O_3 - P_2O_5 - SiO_2$ , hence a nonconductive oxide) for the aforementioned at nonconductive oxide layers 62, and to select germanium borophospho silicate glass (also a nonconductive oxide) for the aforementioned nonconductive layers 64.

Applicant is reminded in this regard that it has been held that mere selection of known materials generally understood to be suitable to make a device, the selection of the particular material being on the basis of suitability for the intended use, would be entirely obvious. In re Leshin 125 USPQ 416.

9. ***Claim 8 is rejected*** under 35 U.S.C. 103(a) as being unpatentable over Hsia et al (5,827,783) in view of Ando (6,097,053) and Haller et al (5,804,506). With reference to Figs. 7 and 8: Hsia et al teach a semiconductor memory device (cf. column 1, line 6 and column 4, lines 12-13) having at least one memory cell having a capacitor cell (cf. column 2, line 60-62) formed of multiple layers of glass, said capacitor cell having a sidewall surface (cf. Figure 5-8), comprising: at least one capacitor cell 78 (cf. column 6, line 47) having a portion thereof formed by a plurality of layers of nonconductive oxide 62 (cf. column 5, lines 33-35) and a plurality of layers of non-conductive oxide 64 (cf. column 4, line 66 – column 5, line 1), at least a portion of at least one layer of said plurality of layers 64 contacting at least a portion of at least one layer of said plurality of layers of nonconductive oxide 62;

at least one layer 26 (cf. Figure 5 and col. 2, l. 2) of dielectric material (polysilicon is a dielectric material) covering at least the sidewall surface of the said capacitor cell; and

at least one electrode layer 28 (cf. col. 2, l. 1-11) deposited over at least a portion of the at least one layer of dielectric material.

*Hsia et al do not necessarily teach* the nonconductive oxide layers 62 to be boro-phospho silicate glass and the nonconductive oxide layers 64 to be germanium boro-phospho silicate glass. However, the use of boro-phospho silicate glass (BPSG) is a standard choice for the capacitor side walls in the semiconductor device art as evidenced by the description of the prior art in Ando (cf. Figure 4, col. 2, l. 1-14), while

BPSG is widely known to be advantageous for its ease of deposition at relatively low temperature, reduced stress, and relatively low glass flow temperatures. Furthermore, it has been known for years that germanium doping of boro-phospho silicate glass markedly increases the etch rate (both wet and dry) of boro-phospho silicate glass, as witnessed by Haller (Abstract, fifth and sixth sentence; column 2, lines 65-67, and column 3, lines 17-24; cf. also Figs. 2 and 3).

*Therefore, it would have been obvious* to one of ordinary skills in the art to modify the invention by Hsia et al at the time it was made so as to select boro-phospho silicate glass ( $B_2O_3 - P_2O_5 - SiO_2$ , hence a nonconductive oxide) for the aforementioned at nonconductive oxide layers 62, and to select germanium boro-phospho silicate glass (also a nonconductive oxide) for the aforementioned nonconductive layers 64.

Applicant is reminded in this regard that it has been held that mere selection of known materials generally understood to be suitable to make a device, the selection of the particular material being on the basis of suitability for the intended use, would be entirely obvious. In re Leshin 125 USPQ 416.

10. **Claims 9** is rejected under 35 U.S.C. 103(a) as being unpatentable over Hsia et al (5,827,783) in view of Ando (6,097,053) and Haller et al (5,804,506). With reference to Figs. 7 and 8: Hsia et al teach a semiconductor memory device (cf. column 1, line 6 and column 4, lines 12-13) having at least one memory cell having a capacitor cell (cf. column 2, line 60-62) formed of multiple layers of glass, said capacitor cell having a sidewall surface (cf. Figure 5-8), comprising: at least one capacitor cell 78 (cf. column 6,

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line 47) having a portion thereof formed by a plurality of layers of nonconductive oxide 62 (cf. column 5, lines 33-35) and a plurality of layers of non-conductive oxide 64 (cf. column 4, line 66 – column 5, line 1), each layer of 64 having at least a portion thereof contacting at least a portion thereof contacting of at least one layer of said plurality of layers 64 contacting at least a portion of at least one layer of said plurality of layers 62;

at least one layer 26 (cf. Figure 5 and col. 2, l. 2) of dielectric material (polysilicon is a dielectric material) covering at least the sidewall surface of the said capacitor cell; and

at least one electrode layer 28 (cf. col. 2, l. 1-11) deposited over at least a portion of the at least one layer of dielectric material.

*Hsia et al do not necessarily teach* the nonconductive oxide layers 62 to be borophospho silicate glass and the nonconductive oxide layers 64 to be germanium borophospho silicate glass. However, the use of borophospho silicate glass (BPSG) is a standard choice for the capacitor side wall material in the semiconductor device art as evidenced by the description of the prior art in Ando, while BPSG is widely known to be advantageous because of ease of deposition at relatively low temperature, reduced stress, and relatively low glass flow temperatures. Furthermore, it has been known for years that germanium doping of borophospho silicate glass markedly increases the etch rate (both wet and dry) of borophospho silicate glass, as witnessed by Haller (Abstract, fifth and sixth sentence; column 2, lines 65-67, and column 3, lines 17-24; cf. also Figs. 2 and 3).

*Therefore, it would have been obvious* to one of ordinary skills in the art to modify the invention by Hsia et al at the time it was made so as to select boro-phospho silicate glass ( $B_2O_3 - P_2O_5 - SiO_2$ , hence a nonconductive oxide) for the aforementioned at nonconductive oxide layers 62, and to select germanium boro-phospho silicate glass (also a nonconductive oxide) for the aforementioned nonconductive layers 64.

Applicant is reminded in this regard that it has been held that mere selection of known materials generally understood to be suitable to make a device, the selection of the particular material being on the basis of suitability for the intended use, would be entirely obvious. In re Leshin 125 USPQ 416.

11. ***Claim 11*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Hsia et al, Ando, and Haller et al as applied to claim 9 above, and further in view of Kawakubo (5,889,696). As detailed above, claim 9 (on which claim 11 depends) is unpatentable over Hsia et al in view of Ando and Haller et al, neither of whom, however, specifically teach the semiconductor memory device of claim 9 with the further limitation as defined by claim 11.

*However, particularly the use of BST as a high dielectric in capacitors* in semiconductor memory devices has long been taught as a means to increase the charge storage capacity of capacitors, as witnessed, for example, by Kawakubo et al, who teach a semiconductor memory device (cf. Abstract, first sentence) with capacitor (cf. Abstract, first sentence) *for the very purpose of achieving very high charge storage ability through the very high dielectric constant of BST* (cf. column 9, lines 58-63).

*Therefore, it would have been obvious* to one of ordinary skills in the art to modify the invention by Hsia et al at the time it was made so as to include the further limitation of claim 11.

12. ***Claim 12*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Hsia et al, Ando, and Haller et al as applied to claim 9 above, and further in view of De Boer et al (5,930,106 and DERWENT copy, under "Novelty"). As detailed above, claim 9 (on which claim 12 depends) is unpatentable over Hsia et al in view of Ando and Haller et al, who, however, do not specifically teach the conductive layer to comprise Si-Ge.

However, Si-Ge has long been taught as semiconductor memory device capacitor electrode material for the purpose of high reliability, as evidenced by De Boer et al, who teach a Si-Ge capacitor plate for the purpose of achieving high reliability (cf. particularly the DERWENT SUMMARY of De Boer et al) in a semiconductor memory device capacitor (cf. Abstract, final sentence; column 2, lines 24-28). Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention of Hsia et al at the time it was made so as to include the further limitation of claim 12.

### ***Conclusion***

1. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

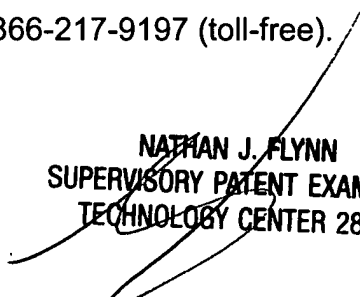
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mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
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May 4, 2004